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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/587,287

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Aaron Reel Bouillet

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EXAMINER

LUGO, DAVID B

ART UNIT

PAPER NUMBER

2611

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/587,287	Applicant(s) BOUILLET, AARON REEL	
	Examiner DAVID B. LUGO	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-10 is/are allowed.
- 6) ☒ Claim(s) 1-6 and 11-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 July 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>7/25/06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 115, 125 (page 4, line 5). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:
3. Page 7, line 11, "250, 255" should be "450, 455".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

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international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5, 11, 12 and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by McNeely U.S. Patent No. 4,814,879 (cited by Applicant).

6. Regarding claims 1 and 11, McNeely discloses an apparatus in Figure 2 comprising a source of a first clock signal 210, a source of a second clock signal 212, delay means (22-28) comprising a plurality of outputs for delaying the first clock signal responsive to the second clock signal, and comparing means (240-248) for comparing two or more of the outputs to produce a first output signal.

7. Regarding claim 2, the first output signal produced (CLK') is a synchronization of the first input signal and the second input signal.

8. Regarding claims 3 and 14, the first clock signal 210 is a fixed rate clock signal (col. 6, lines 48-49), and the second clock signal 212 is a clock signal derived from a PLL (col. 4, lines 35-39).

9. Regarding claims 4 and 15, the delay means (22-28) comprises a plurality of flip-flops (see Fig. 2).

10. Regarding claims 5 and 16, a plurality of comparisons are made between a plurality of the outputs of the delay means via gates 240-248 to produce multiple output signals (see Fig. 2).

11. Regarding 12, McNeely shows that comparing of two or more of the plurality of outputs of the delay means are is performed using logic devices (240-248 – see Fig. 2).

12. Claims 1, 2 and 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuwata et al. U.S. Patent No. 2004/0062336.

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13. Regarding claim 1, Kuwata discloses an apparatus in Figure 2 comprising a source of a first input signal (1), a source of a second input signal (2), a delay means (41-44) comprising a plurality of outputs (3-6) for delaying the first input signal responsive to the second input signal, and a means (45-47) to compare the plurality of outputs of the delay means to produce a first output signal.

14. Regarding claim 2, the output signal is a synchronization of the first input signal and the second input signal as the falling edge of output signal 2 coincides with the changing edge of the signal 1 (para. 0014).

15. Regarding claim 4, the delay means (41-44) comprises a plurality of flip flops.

16. Regarding claim 5, a plurality of comparisons are made between a plurality of the outputs of the delay means to produce multiple output signals 7, 8.

17. Regarding claim 6, the output signal (CLKout) is a clock signal with a 50% duty cycle (see Fig. 4).

18. Claims 1-4, 6, 11, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito U.S. Patent Application Publication No. 2003/0117190.

19. Regarding claims 1 and 11, Ito discloses an apparatus in Figure 1 comprising a source of an input clock signal (ICLK), a source of a second input clock signal (RCLK), a delay means (11, 1R, 3) comprising a plurality of outputs for delaying the first clock signal responsive to the second clock signal, and means for comparing (10) two or more of the outputs of the delay means to produce an output signal.

20. Regarding claim 2, the first output signal produced is a synchronization of the first input signal and the second input signal (para. 0041).

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21. Regarding claims 3 and 14, the first clock signal (ICLK) is a fixed clock rate signal (see Fig. 16), and the second clock signal is derived from PLL 10 (see Fig. 1, para. 0041).

22. Regarding claims 4 and 15, Ito further discloses that the delay means comprises a plurality of flip flops (see Fig. 9).

23. Regarding claim 6, the output signal is a clock signal with a 50% duty cycle (see Fig. 16).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

25. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Renner et al. U.S. Patent Application Publication No. 2005/0007493.

26. Regarding claims 12 and 13, Ito discloses a method for synchronizing a first clock signal and a second clock signal as described above, where a PLL is used to compare the outputs of delay means is indicated as having a conventional configuration (see para. 0060, Fig. 1). Ito does not expressly disclose that the PLL used in the comparing is implemented using logic devices or software.

27. Renner teaches that a PLL may be implemented in hardware or software (para. 0016).

Further, implementing a PLL in hardware using logic devices is well known in the art.

Accordingly, it would have been obvious to one of ordinary skill in the art to implement the comparing device (i.e. PLL) of Ito using logic devices or software as a matter of design consideration, as both will function to provide the desired output.

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Allowable Subject Matter

28. Claims 7-10 are allowed.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Chien U.S. Patent No. 7,170,965 discloses a frequency divider with a plurality of flip-flops in Figure 4.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID B. LUGO whose telephone number is (571)272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3066. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David B. Lugo/
Primary Examiner, Art Unit 2611
6/18/09